CSE464/ELE464: Intro to VLSI Design

SYLLABUS FALL-2012

Instructor

Professor Qinru Qiu, Department of Electrical Engineering and Computer Science, Room CST 4-281,
Tel: (315)443-1836, email: qiqiu@syr.edu
Office Hours: Tuesday 11:30am – 3:30pm

Class Location and Times (Lectures)

Day: Monday & Wednesday
Location: SCITC 1-242
Time: 10:35am ~ 11:55am

Class Location and Times (Recitation)

Day: Friday
Location: SCITC 1-242
Time: 11:40aM ~ 12:35pM

Books

- (*Required*) Textbook: J. M. Rabaey, A. Chandrakasan, and B. Nikolic, "Digital Integrated Circuits: a Design Perspective", 2nd edition, Prentice Hall 2003
- (*Optional*) Reference: N. H. E. Weste and D. Harris, "CMOS VLSI Design: A Circuits and Systems Perspective", 4th edition, Addison-Wesley, 2010

Course Web Page

All instructional materials, including lecture notes, homework and lab assignments will be posted on BlackBoard@SU. Look for Blackboard announcement for important messages.

Description

The goal of this course is to study the process of implementing a digital system as a CMOS integrated circuit.

The course will begin with a review of the basics of CMOS transistor operation and the manufacturing process for CMOS VLSI chips. We will then study in detail the problem of implementing logic gates in CMOS. Specifically, we will cover layout, design rules and circuit families. Afterwards, we will examine techniques for analyzing and optimizing timing and power at the circuit level. We will study sequential elements – latches and flops – and clocking. This will be followed by a discussion of datapath design: detection logic, shifters, comparators, adders and multipliers. We will also study memories; specifically the workhorse 6-T SRAM cell as well as the peripheral decode logic.

(Technical Elective Course; Prerequisites: CSE 381, CSE 398, ELE331)

Learning outcomes

After taking this course, the students should be able to:

1. Understand the functions and the properties of CMOS devices, combinational gates, and sequential circuits
2. Analyze the performance and power consumption of a digital VLSI circuit using proper device and interconnect models
3. Design functional units such as adders and multipliers using CMOS devices

4. Optimize a digital circuit with respect to different quality metrics such as cost, speed, power dissipation, and reliability
5. Use Cadence layout design and simulation tool for VLSI circuit design and analysis

Topics covered

1. Introductions
2. CMOS devices
3. The manufacturing process
4. Wire modeling
5. CMOS inverter
6. Combinational logic gates
7. Datapath design
8. Sequential logic gates
9. Digital circuit timing analysis
10. Designing Memory blocks

Grading policy

Labs: 20%
Final Project: 20%
Homework: 30%
Midterm Exam: 30%

Grading Scale:

90 ~ 100 = As
80 ~ 89 = Bs
70 ~ 79 = Cs
60 ~ 69 = D
Below 60 = F

Homework Policy

Homework assignments are to be submitted through Blackboard website or hand to the instructor on the assignment due date. Assignments submitted after the due date will be deducted 10 points for each day late.

Exams

All exams must be taken at the scheduled time unless a previous arrangement (with a good reason) has been made with the instructor

Attendance

You are expected to attend each class punctually and remain for the entire class period. You need to inform the instructor in advance if you expect to miss a class or leave the course before the end of the semester. If you miss class your absence will be excused by the instructor only if a doctor's certificate or other evidence is submitted. You remain to be responsible for the work associated with the class you missed, even if your absence has a valid reason. There will be a number of unannounced popup quizzes during the semester.

Academic Honesty

Cheating in any form is not tolerated, nor is assisting another person to cheat. The submission of any work by a student is taken as a guarantee that the thoughts and expressions in it are the students own except when properly credited to another.

Violations of this principle include giving or receiving aid in an exam or where otherwise prohibited, fraud, plagiarism, the falsification or forgery of any record, and any other deceptive act in connection with

academic work. Plagiarism is the representation of another's words, ideas, programs, formulae, options or other products of work as one's own work from others, since it is often not possible to determine who the originator or the copier was. Such offense will result in a failing grade "F" and a letter of reprimand in your department student file.

Course calendar

Week	Material
Week 1 ~ Week 2 (8/27~9/07)	Introduction CMOS devices Lab 0
Week 3 ~ Week 5 (9/10~ 9/28)	Manufacturing process, Wire Model CMOS inverter Lab 1
Week 6 ~ Week 8 (10/01~10/19)	Combinational gates Lab 2
Week 9 ~ Week 10 (10/22 ~ 11/02)	Datapath Design project kickoff Lab 3
Week 11 ~ Week 12 (11/05~11/16)	Sequential Circuit and timing analysis Lab 4, Lab 5
Week 13 ~ Week 14 (11/19~12/07)	Memory design

Note: The schedule might change during the semester depending on the progress of the class. All departmental, college and university regulation regarding class attendance, course drop, etc will be followed.

Contribution to Student Learning Outcomes:

a) an ability to apply knowledge of mathematics, science, and engineering.	**M**
b) an ability to design and conduct experiments, as well as to analyze and interpret data.	**S**
c) an ability to design a system, component, or process to meet desired needs within realistic constraints such as economic, environmental, social, political, ethical, health and safety, manufacturability, and sustainability.	**S**
d) an ability to function on multidisciplinary teams.	**M**
e) an ability to identify, formulate, and solve engineering problems.	**S**
f) an understanding of professional and ethical responsibility.	**W**
g) an ability to communicate effectively.	**M**
h) the broad education necessary to understand the impact of engineering solutions in a global, economic, environmental, and societal context.	**W**
i) a recognition of the need for, and an ability to engage in life-long learning.	**W**
j) a knowledge of contemporary issues.	**S**
k) an ability to use the techniques, skills, and modern engineering tools necessary	**S**

for engineering practice.	
l) an ability to verify design correctness and evaluate performance of computing systems.	**S**