Design Considerations for Digital Circuits Using Organic Thin Film Transistors on a Flexible Substrate

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Abstract— Organic Thin Film Transistor (OTFT) is the basic device for building analog and digital circuits and systems on a flexible substrate. Our studies show that, complementary design logic (CMOS), which is most common in MOSFET circuit design, is not suitable for OTFT circuits. In this work, we propose a new design logic that fits the characteristics of OTFT devices. Considering the fact that the mobility of the ptype OTFT is much better than the n-type OTFT, the proposed design logic uses mostly p-type OTFTs to implement logic functions. Circuit simulations have been done to compare the proposed design logic with other existing ones. The results show that the proposed design logic can improve the performance of the circuit by 2~4X, lower the energy dissipation by 2~6X, and reduce the circuit area by 2~10X.

I. INTRODUCTION

Flexible electronics is a new technology for building electronic circuits by depositing electronic devices on flexible substrates such as plastic, paper, or even cloth. Compared with silicon-based electronics, flexible electronics has the following advantages. First of all, it can take variable forms for different applications; secondly it is thin, light weight, and unbreakable; thirdly it is low-cost due to cheaper material and cheaper manufacturing processes; finally it can be produced for large-area applications.

Two of the often-discussed application drivers for flexible electronics are: radio-frequency identification (RFID) tags and large area flexible display. An ultra-lowcost all-printed RFID system is under research and development at University of California Berkeley [1]. A prototype of the roll-able display is a joint research work of the Army Research Laboratory and the Arizona State University [2]. The most advanced digital application of flexible electronics, that has been reported, is the 8-bit flexible microprocessor by Epson, which consists of about 32,000 transistors and weighs only 140 milligrams. Flexible digital and analog integrated circuits could also be the key technology to design some important system components of wearable computers [4].

To build digital and analog integrated circuits on a flexible substrate, such as plastic, a whole new class of basic devices is needed. Traditional crystalline silicon-based semiconductor (it will be referred as MOSFET for the remaining parts of the paper) devices and manufacturing process is not suitable for flexible substrates. Instead, it requires devices based on organic semiconductors [5]-[7] and corresponding manufacturing process. Over the past two decades, a tremendous amount of research work has been done in search of organic semiconductor materials [5][7]. The formal name of the transistors made from these materials is the Organic Thin Film Transistors (OTFTs).

Methodologies for circuit design and optimization are crucial for closing the gap between devices and real practical applications of OTFT flexible electronics. Efforts in building experimental digital integrated circuits using OTFT have been carried out, but in very limited number and small scale [9]-[12]. Reported designs used the same circuit design approaches as in MOSFET circuits and did not look at how to make improvements in performance, power, area or reliability.

In this research work, we propose a new type of design logic that fits the characteristics of the OTFT devices. The proposed design logic uses mostly the p-type OTFTs to implement logic functions, by considering the fact that the mobility of the p-type OTFT is 30 to 50 times better than the n-type OTFT. Circuit simulations have been done to compare the proposed method with existing design logics such as the complementary logic (CMOS) and the Pseudo-PMOS logic. Experimental results show significant improvements in performance, power and area by the proposed method.

The rest of the paper is organized as follows. Section II gives the background on OTFT device and simulation model. The proposed design logic and experimental results are presented in Section III. Section IV summarizes the work.

II. BACKGROUND

A. MOSFET versus OTFT

Figure 1(a) shows the basic structure of a p-type MOSFET and its typical I-V curves [17]. Figure 1(b) shows the basic structure of a p-type OTFT and its typical I-V curves [14]. In terms of the similarities and differences

between MOSFET and OTFT, it is not possible to have every detail aspect (chemical, mechanical and electrical) discussed here. For the scope of this work, the similarities can be summarized as follows.

1. They are both field effect transistors, meaning that they are used as switches whose on/off state is controlled by the electric field across the channel, i.e., the voltage difference between the "gate" and the "source".

2. They have similar shapes and behavioral trends in their IV curves, meaning that they have similar working mechanism and electrical characteristics as switches.

3. There are two basic device classes for both of them: n-type which transports charges by electrons; and p-type which transports charges by holes.



Figure 1 Basic structures and I-V curves of MOSFET and OTFT.

The differences between MOSFET and OTFT can be summarized as follows.

1. The (field effect) mobility of the best known OTFT (p-type) is about 1~2 cm2/V-s [5][6][7], the mobility of the state-of-the-art MOSFET (n-type) is about 400~500 cm2/V-s [17][18], which is about 200 to 500 times better than OTFT. Since the performance of a transistor (mainly switching speed) is basically proportional to its mobility, the performance of the circuits using OTFT is expected to be at least two (even three) orders of magnitude worse than the ones using MOSFET.

2. For MOSFET, the mobility of the n-type transistor is about 2 to 3 times better than the p-type transistor. For OTFT, the mobility of the best-known feasible n-type transistor (nOTFT) is about 30 to 50 times worse than the ptype transistor (pOTFT), in spite of the extensive material research in both types of transistors. Furthermore, research results show that the material choices for the n-type OTFT are far more limited than the choices for the p-type OTFT, and most n-type materials either are unstable in ambient conditions or have poor mobility [5][6][7].

3. For MOSFET, the supply voltage is normally between 1.2V to 2.5V. For OTFT, the supply voltage is normally between 5V to 50V (typically at about 25V for mature technology) [6][14][15].

B. Device models

Pentacene is regarded as the best material for pOTFT by many device researchers [5]-[7]. During this study, the pentacene-based OTFT reported in [14] has been chosen as the basic targeting device.

In supporting the proposed approach, some circuit simulation results using the HSPICE [16] circuit simulator will be discussed. Since there are no existing SPICE models for OTFT devices, a SPICE model of the pOTFT is built using the parameters (mobility, threshold voltage, thickness of dielectric layer, etc.) reported by [14]. We then derive the SPICE model of the nOTFT based on the pOTFT model by reducing the mobility by a factor of 40 and using a positive threshold voltage [5]-[7]. The correctness of the models has been verified by generating the I-V curves using simulation and comparing them with the measured I-V curves in [14].

For the purpose of easier presentation and more intuitive connection with traditional circuit terminologies, we will use "PMOS" when referring to either p-type MOSFET or p-type OTFT and "NMOS" when referring to either n-type MOSFET or n-type OTFT, unless stated specifically.

III. THE PMOS-ONLY PRE-DISCHARGED DESIGN LOGIC

A. Basic circuit structure

For design logic that only uses PMOS transistors, the *Pseudo-PMOS* logic fits the requirement. It replaces the pull-down network (NMOS transistors) in a complementary logic gate with a single weak PMOS transistor. A new design logic is invented based on the principles of dynamic logic [17]. We named it the *PMOS-Only Pre-Discharge* logic, or simply "POPD logic".

Studies have been done to evaluate the following four design logic options in designing digital circuits using OTFTs. 1). Strength-Matched CMOS; 2). Strength-Unmatched CMOS; 3). Pseudo-PMOS; 4). POPD. Figure 2 shows the implementations of the inverter using different options.

The working mechanism of the POPD logic consists of two phases: "discharge" and "evaluate". In the discharge phase, CLK = '0', the "discharge" PMOS is on, thus the output Y = '0', independent of the logic value of input A. In the evaluate phase, CLK = '1', the "evaluate" PMOS is on, thus output Y will evaluate the implemented logic, depending on the input logic value(s). Note that Y will only discharge to V_{th} , where (- V_{th}) is the threshold voltage of the PMOS. However, if the V_{th} is small enough, it is still regarded as logic '0'.

All four inverters are simulated by setting $W_p = 240\mu m$, $W_{pull-down} = 44\mu m$, $W_{discharge} = 240\mu m$, $W_{evaluate} = 240\mu m$. Same channel length ($L = 44\mu m$ [14]) is used for all transistors and the same periodical input waveform for the inputs. A capacitor of capacitance (C = 10pF) is connected to the output of each inverter.



Figure 2 Implementations of an inverter gate. (a) Strength-Matched CMOS; (b) Strength-Unmatched CMOS; (c) Pseudo-PMOS; (d) POPD

 Table 1 Performance, power and area comparisons for inverters in Figure 2.

	Rise	Fall	Avg.	Power	Total
	Delay	Delay	Delay	(μW)	Width
	(μs)	(μs)	(μs)		(μm)
Fig. 1(a)	232.1	122.6	177.4	30.0	9840
Fig. 1(b)	88.0	197.5	142.8	10.5	2640
Fig. 1(c)	21.0	175.5	98.3	20.0	764
Fig. 1(d)	41.0	55.7	48.4	5.0	720

Performance and power results are obtained from HSPICE simulations. Table 1 shows the rise delay, fall delay, average delay, power consumption and area (in terms of total transistor width) values for all implementations. Note that the delay of the POPD inverter is measured with respect to the rising edge of the "CLK" signal.

Similar trends are observed for other basic logic gates such as NAND, NOR and XOR. The experimental results show that,

1. Strength-Matched CMOS logic is the worst in every category. Although it is expected to have the best performance, the strength matching requirement leads to NMOS transistors with excessively large sizes. This causes severe input-output coupling effects in the simulation, resulting in bad performance and power.

2. Strength-Unmatched CMOS logic is good for power, but provides bad performance. The circuit area is large, but may be acceptable with smaller device feature size in the future. To build circuits with good performance, the use of it should be avoided or minimized.

3. Pseudo-PMOS logic is good for performance and area in overall. The fall delay is not satisfying, due to the fact that it must have a weak pull-down transistor. Because of the standby current, which does not exist in other three implementations, Pseudo-PMOS logic is not good for low power design purposes.

4. POPD logic demonstrates the best performance, power and area. Although there is timing overhead for discharge time, it can be easily removed by advanced design techniques such as the 2-phase domino pipeline.

B. Design method for large circuits

After the study of the basic logic gate designs, further study on design methodologies for larger, more complex combinational circuits is done. During this process it is found that POPD gates cannot be used alone to implement combinational circuits. POPD logic belongs to the category of dynamic logic. To make dynamic logic circuit work reliably, it is required that, the output of a dynamic gate, must go through an inverting static gate (such as a static inverter), before it can be connected as the input of another dynamic gate [17]. Therefore, a static logic should be chosen, either CMOS or Pseudo-PMOS, to be used with POPD logic.

An 8-bit ripple-carry adder is used to study the following five design options: 1) Strength-Matched CMOS; 2) Strength-Unmatched CMOS; 3) Pseudo-PMOS; 4) POPD with Strength-Unmatched CMOS inverters; 5) POPD with Pseudo-PMOS inverters.

Figure 4 shows the schematic of the circuits for AND, OR and XOR logic functions for options 4 and 5. The inverters with symbol "N" are normal inverters and implemented as in Figure 2(b) for option 4, as in Figure 2(c) for option 5. The inverters with symbol "G" are the "guard inverters" for dynamic circuits [17]. They are implemented using complementary logic with $W_p = 120\mu m$ and $W_n = 240\mu m$. In case that the n-type OTFT is not available, the guard inverters can be removed, taking risks of charge sharing and charge leakage [17]. However these risks can be minimized by careful design efforts.

Table 2 shows the comparison of worst-case delay, average energy dissipation per operation using randomly generated input vectors, and area (in terms of total transistor width).

The simulation results of the adder designs show that,

1. Strength-Matched CMOS, which is used by most MOSFET circuits, is not feasible for OTFT circuits.

2. The observations for Strength-Unmatched CMOS and pseudo-PMOS are similar to the ones from the single gate simulations.

3. POPD with Pseudo-PMOS inverters and POPD with Strength-Unmatched CMOS inverters design options achieve similar good results in performance. While the former has better area and the latter has better power.



Figure 4 Circuit schematics of the AND, OR and XOR functions.

 Table 2 Comparisons of performance, power and area for five adder designs.

	Opt. 1	Opt. 2	Opt. 3	Opt. 4	Opt. 5
Worst-case delay (ms)	37.1	22.1	6.0	0.8	1.0
Energy per operation (μJ)	12.2	3.6	20.0	2.1	5.3
Total transistor width (<i>m</i>)	3.38	0.96	0.24	0.32	0.16

Initial simulation results demonstrate that POPD logic is the best solution to digital circuit design using OTFTs, for the best performance, power and area. POPD with Pseudo-PMOS inverters and POPD with CMOS inverters are both good candidates for design of large circuits. There will be cases when it is desirable to use only p-type OTFTs in the entire design, due to availability, reliability or manufacturing concerns. Then the design method that uses POPD gates with Pseudo-PMOS inverters should be the primary choice.

IV. CONCLUSIONS

In this paper, we have proposed a new design method for digital circuits and systems using the organic thin film transistors on a flexible substrate. Experimental results show that the proposed method improves performance, power and area, when compared with existing design logics.

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