# A Probabilistic Technique for Full-chip Leakage Estimation

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**ABSTRACT** – In this paper, we propose a probability-based algorithm to estimate full-chip leakage without knowing layout information, under intra-die and inter-die process variations. Through modeling process variations into a random vector, we show that the standard cell leakage can be modeled as an inverse Gaussian random variable and further demonstrate that full-chip leakage can also be approximated to be an inverse Gaussian random variable. Hence, the leakage estimation problem is reduced to the estimation of the mean value and variance of the full-chip leakage. Experimental results show that the proposed algorithm is over 1000X faster than Monte Carlo simulation while the maximum estimation error is less than 6%.

**Categories and Subject Descriptors:** B.8.2 [Hardware]: Performance and Reliability--Performance Analysis and Design Aids

**General Terms:** Algorithm, design, performance, reliability

**Keywords**: VLSI, leakage estimation

## 1. Introduction

Leakage power consumption rises as a major issue in the nano-scale circuit design. It primarily consists of subthreshold leakage and gate tunneling leakage [2]. Due to process variations, these two components are nondeterministic. That makes the full-chip leakage a random variable, and increases difficulties to estimate the full-chip leakage and to capture its features.

Leakage power's sensitivity to process variations increases much difficulty to estimate the total leakage of a chip. So far many works [4, 6-12] have been presented to estimate the total leakage, taking into account the intra-die variation and inter-die variation. The full-chip leakage is approximated by a log-normal random variable in most of these works. In order to make full-chip leakage subject to a log-normal distribution, a first-order Taylor expansion is used in their derivations. However, the process variation could be quite large in nano-scale CMOS technology and leakage current dose not linearly depend on the process variation, so the linear approximation leads to inaccurate results. In [12], a quadratic model is used to improve the accuracy of results.

However, there are two common limitations existing in these algorithms for leakage estimation

1. The leakage estimation can be done only after the layout information of circuit design is available.
2. For large circuits, these algorithms could be prohibitively expensive in terms of computation complexity.

A random-gate-based leakage estimation technique in [13] is proposed to overcome these two problems. This work assessed the mean and variance of full-chip leakage before the layout. But it did not provide the leakage distribution. Furthermore, the work in [13] did not consider the leakage component caused by gate tunneling, which contributes a significant part to the total leakage.

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In order to overcome the limitations stated above, we propose a novel probabilistic technique for full-chip leakage estimation in this paper.

The highlights of this paper are as follows:

1. We have derived a universal model to represent process variations.
2. We take into account the gate tunneling leakage component when estimating full-chip leakage
3. We have derived that the full-chip leakage follows an inverse Gaussian
4. The approach largely reduces the computation time for full chip leakage estimation

## 2. Modeling

### 2.1 Process Variations

Process variations are categorized into *intra-die process variation* and *inter-die process variation*, and they are mutually independent. Intra-die process variations are limited to a die. These variations are spatially correlated and are represented by an $N$×1 column random vector $\mathbf{x}_{\text{intra}} = (x_1, x_2, ..., x_n, ..., x_N)^t$, where $x_n (1 \le n \le N)$ are random variables, each representing one of intra-die parameter variations; $N$ is the number of parameters that suffer from process variations; and symbol "$t$" means matrix transpose operation. The different gates on the same die will have different realizations of random vector $\mathbf{x}_{\text{intra}}$ such as $\mathbf{x}^i_{\text{intra}} = (x^i_1, x^i_2, \cdots, x^i_N)^t$ for gate $i$ and $\mathbf{x}^j_{\text{intra}} = (x^j_1, x^j_2, \cdots, x^j_N)^t$ for gate $j$.

Intra-die variations indicate transistors located in the proximity are more likely to have similar characteristics than transistors far away from each other, and this property is captured by the component correlations between $\mathbf{x}^i_{\text{intra}}$ and $\mathbf{x}^j_{\text{intra}}$. We first look at the correlation between components $x^i_m$ and $x^j_n$ from $\mathbf{x}^i_{\text{intra}}$, $\mathbf{x}^j_{\text{intra}}$, where $1 \le m \le N$ and $1 \le n \le N$. If $m$ is not equal to $n$, $x^i_m$ represents a different type of parameter variation from $x^i_n$, then,

$$\rho_{x^i_m, x^j_n} = 0, \qquad \text{if } m \ne n,\ i \ne j \tag{1}$$

If $m$ is equal to $n$, $x^i_m$ and $x^j_n$ both represent the same type of parameter variation, then correlation coefficient $\rho_{x^i_m, x^j_n}$ between them is determined by the distance between gate $i$ and gate $j$ in the layout, that is

$$\rho_{x^i_m, x^j_n} = f(d), \tag{2}$$

where $d$ is the distance between gate $i$ and gate $j$, $f(\bullet)$ is a monotonically decreasing function from $A \subset R \to [0,1]$, and $A$ is defined as

$$A := \{d;\ d \text{ is the distance between any two gates in layout}\}.$$

As $d$ goes to 0, the correlation coefficient $\rho_{x^i_m, x^j_n}$ goes to 1; as $d$ goes larger and larger, $\rho_{x^i_m, x^j_n}$ turns out to be smaller and smaller, and eventually becomes 0. Function $f(\bullet)$ is determined by the manufacturing process for a specific chip.

Putting equations (1) and (2) together, the correlation coefficient $\rho_{x_m^i,x_n^j}$ is represented by,

$$\rho_{x_m^i,x_n^j} = \begin{cases} 0 & if\ m \neq n, i \neq j \\ f(d) & if\ m = n \end{cases}, \quad (3)$$

Inter-die process variations are variations across dies, and it affects all transistors on the same chip, e.g., making gate oxide thickness of all transistors larger or smaller than the nominal value. Similarly, it is also represented by a $N\times1$ column random vector $\mathbf{x}_{\text{inter}} = (x_{N+1}, x_{N+2}, ..., x_{N+n}, ..., x_{N+N})^t$, where $x_{N+n}(1 \le n \le N)$ are random variables, and each of them represents one of the inter-die parameter variations, all gates on the same die share the same realization of random vector $\mathbf{x}_{\text{inter}}$. If we stack the intra-die variation and inter-die variation together, then the overall variation is expressed by a new $2N\times1$ column random vector named *process random vector*,

$$\mathbf{x}_{\text{variation}} = (\mathbf{x}^t_{\text{intra}}\ \mathbf{x}^t_{\text{inter}})^t \quad (4)$$

It is obvious that all components in $\mathbf{x}_{\text{variation}}$ are mutually independent.

The overall variation in gate $i$ is fully captured by a $2N\times1$ column random vector $\mathbf{x}^i_{\text{variation}}$, which is shown as,

$$\mathbf{x}^i_{\text{variation}} = (x_1^i, x_2^i, \cdots, x_N^i, x_{N+1}, \cdots, x_{N+N})^t \quad (5)$$

Similarly, overall variation in gate $j$ is fully described by a $2N\times1$ column random vector $\mathbf{x}^j_{\text{variation}}$, which is

$$\mathbf{x}^j_{\text{variation}} = (x_1^j, x_2^j, \cdots, x_N^j, x_{N+1}, \cdots, x_{N+N})^t \quad (6)$$

Note that the last $N$ components in $\mathbf{x}^i_{\text{variation}}$ and $\mathbf{x}^j_{\text{variation}}$ are the same; it is because these $N$ components represent the inter-die variations, and all gates in the same die share the identical inter-die variations.

## 2.2 Standard Cell Leakage

The full-chip leakage is simply the summation of the leakage from individual gates across dies. Every gate is drawn from a standard cell library, and it can be regarded as an instantiation of the correspondent standard cell. So first of all, we need study the leakage statistics from a standard cell under process variations.

Given the input pattern, the leakage $L$(g) in a standard cell $g$ can be modeled as a function of process variation, shown as

$$L(\text{g}) = h(\mathbf{x}_{\text{variation}}) \quad (7)$$

where $h(\bullet)$ is a function from $R^{2N} \rightarrow R^+$.

We also use a quadratic model of parameter variation $\mathbf{x}_{\text{variation}}$ to approximate $\log(h(\bullet))$, that is

$$\log(L(g)) = \mathbf{x}^t_{\text{variation}}\mathbf{A}\mathbf{x}_{\text{variation}} + \mathbf{b}^t\mathbf{x}_{\text{variation}} + c \quad (8a)$$

where $\mathbf{A}$ is a $2N\times2N$ diagonal matrix, $\mathbf{b}$ is a $2N\times1$ column vector, and $c$ is a scalar constant. $\mathbf{A}$, $\mathbf{b}$, $c$ are determined by curve fitting.

We also point out that for different standard cells, $\mathbf{A}$, $\mathbf{b}$, $c$ will be different. In order to apparently show that A, b, c depend on standard cell type, we rewrite equation (8a) as,

$$\log(L(g)) = \mathbf{x}^t_{\text{variation}}\mathbf{A}(g)\mathbf{x}_{\text{variation}} + (\mathbf{b}(g))^t\mathbf{x}_{\text{variation}} + c(g) \quad (8b)$$

where the meanings of $\mathbf{A}(g)$, $\mathbf{b}(g)$ and $c(g)$ are self-explanatory.

For the sake of convenience, equation (8a) is used instead of equation (8b) if there does not exist confusion in the context about the meaning of $\mathbf{A}$, $\mathbf{b}$, $c$. Based on equation (8), the mean $\mu_g$ and variance $\sigma_g^2$ of the leakage from a standard cell $g$ can be derived under process variations.

In order to make equation (8) more tractable, we define two dummy vectors $\mathbf{y}$ and $\mathbf{e}$, and they are both $2N\times1$ column vectors. Let $\mathbf{y} = \mathbf{x}_{\text{variation}}+\mathbf{e}$, that is

$$\mathbf{x}_{\text{variation}} = \mathbf{y} - \mathbf{e} \quad (9)$$

After some mathematical manipulation, we have

$$\log(L(g)) = \mathbf{y}^t\mathbf{A}\mathbf{y} + c_1 \quad (10)$$

where $\mathbf{e}$ and $c_1$ are determined by the following equalities,

$$\mathbf{e}^t = 1/2\mathbf{b}^t\mathbf{A}^{-1}, \qquad c_1 = c - \mathbf{e}^t\mathbf{A}\mathbf{e}$$

Assuming each component in $\mathbf{x}_{\text{variation}}$ is subject to univariate normal distribution, based on equation (9) we know that each component in $\mathbf{y}$ is also following univariate normal distribution. Hence, $\mathbf{y}^t\mathbf{A}\mathbf{y}$ is subject to a linear combination of $\chi^2$ distributions [15], and $L(g)$ can be approximated to follow an inverse Gaussian distribution [16].

## 2.3 Random Gate Leakage

The VLSI circuit design is usually based on the standard cell library. The standard cell library is a collection of standard cells, and it is defined as

$$lib = \{g_i: 1 \le i \le I\} \quad (11)$$

where $g_i$ represents standard cell $i$, and $I$ is the total number of standard cells in the library.

Each gate in the chip is regarded as an instance of the random gate ($RG$) [13], and the sample space for $RG$ is the standard cell library *lib*. $RG$ is a discrete random variable, the probability $p_i$ that $RG$ is instantiated by standard cell $g_i$, that is $p_i = P(RG = g_i)$, is determined by the ratio of the usage of standard cell $g_i$ to the overall usage of the standard cells. Let the usage of gate $g_i$ be $K_i$, then the overall usage of the standard cells is $\sum_{i=1}^{I} K_i$, and $p_i$ can be calculated as,

$$p_i = P(RG = g_i) = K_i/\Sigma K_i \quad (12)$$

Obviously we have

$$\sum_{i=1}^{I} p_i = 1 \quad (13)$$

We introduce a notation $L(RG)$ to denote the leakage in $RG$. $L(GR)$ is also a random variable, and it has a hierarchy distribution. Through the discussion in section 2.2, we know $L(GR)|GR=g_i$ can be approximated to be an inverse Gaussian distribution, and $RG$ is subject to a known discrete distribution with $P(RG = g_i)$ equal to $p_i$. So the mean $\mu_{RG}$ of $L(RG)$ can be obtained by

$$\mu_{RG} = E(L(RG)) = E(\mu_{g_i}) = \sum_{i=1}^{I} p_i\mu_{g_i} \quad (14)$$

where $\mu_{g_i}$ is the mean value of leakage in standard cell $g_i$, under the process variations.

In order to calculate the variance $\sigma^2_{RG}$ of $L(RG)$, we also need to know the second moment $E(L^2(RG))$ of $L(RG)$, and it is

$$E(L^2(RG)) = E(E(L^2(RG) \mid RG = g_i)) = \sum_{i=1}^{I} \mu^2_{g_i} + \sigma^2_{g_i} \quad (15)$$

Right now we are ready to calculate $\sigma^2_{RG}$

$$\sigma^2_{RG} = \sum_{i=1}^{I} p_i(\mu^2_{g_i} + \sigma^2_{g_i}) - (\sum_{i=1}^{I} p_i\mu_{g_i})^2 \quad (16)$$

## 2.4 Random Gate Leakage Correlation Coefficient

The correlation of the intra-die process variations leads to the correlation between leakages from different gates across the chip.

Let two instances of $RG$ $g_i$ and $g_j$, and leakages from these two instances can be represented by $L(g_i)$ and $L(g_j)$, so the covariance between $L(g_i)$ and $L(g_j)$ is

$$\text{cov}(L(g_i), L(g_j)) = $$

$$\exp((\mathbf{x}^j_{\text{variation}})^t\mathbf{A}(g_i)\mathbf{x}^j_{\text{variation}} + (\mathbf{b}(g_i))^t\mathbf{x}^j_{\text{variation}} + c(g_i))) \quad (17)$$

Accordingly, the covariance between two *RGs* is

$$\text{cov}(L(RG_i), L(RG_j)) = \sum_{j=1}^{I}\sum_{i=1}^{I} p_j p_i \,\text{cov}(L(g_i), L(g_j)) \quad (18)$$

And the correlation coefficient $\rho(L(RG_i), L(RG_j))$ can be easily obtained by

$$\rho(L(RG_i), L(RG_j)) = \text{cov}(L(RG_i), L(RG_j)) / (\sigma_{RG}^2) \quad (19)$$

## 3. Full-chip Leakage Analysis

In our analysis approach, a chip consists of individual gates, and each gate is modeled as a random gate *RG*. Accordingly, the full-chip leakage can be modeled as the summation of the leakage from each random gate. Assuming the full-chip leakage is denoted by $L_{fc}$, then it can be expressed by,

$$L_{fc} = \sum_{RG_k \in lib, k=1}^{K} L(RG_k) \quad (20)$$

where $K$ is the total number of random gates used in the circuit. When the circuit design is given, then $K$ it is actually equal to the overall usage of the standard cells, which is $\Sigma K_i$, so we have $K=\Sigma K_i$.
Based on equation (20), we can also calculate some statistics of full-chip leakage such as mean and variance,

$$E(L_{fc}) = E\left(\sum_{RG_k \in lib, k=1}^{K} L(RG_k)\right) = K\mu_{RG} \quad (21a)$$

$$\text{var}(L_{fc}) = \sigma_{RG}^2 \sum_{i=1}^{K}\sum_{j=1}^{K} \rho(L(RG_i), L(RG_j)) \quad (21b)$$

Before working on deriving the distribution of the leakage, we need to clarify one thing: every random gate *RG* is instantiated by one of standard cells in the design library after synthesis and placement for a given circuit design. So the full-chip leakage is expressed as

$$L_{fc} = \sum_{g_k \in lib, k=1}^{K} L(RG_k = g_k) \quad (22)$$

where gate $g_k$ is the realization of random gate $RG_k$.
We have shown in section 2.2 that $L(RG_k = g_k)$ in equation (22) is subjected to the inverse Gaussian distribution under process variations, and the summation of random variables with inverse Gaussian distribution is still following an inverse Gaussian distribution [16], so $L_{fc}$ is a random variable with the inverse Gaussian distribution, and its probability density function (*pdf*) has the following form with two characteristic parameters $\lambda$ and $\mu$

$$f(x;\mu,\lambda) = \left[\frac{\lambda}{2\pi x^3}\right]^{1/2} \exp\left(\frac{-\lambda(x-\mu)^2}{2\mu^2 x}\right), \quad \text{if } x \ge 0 \quad (23)$$

If a random variable $X$ follows an inverse Gaussian with parameters $\mu$ and $\lambda$, then its mean and variance are $\mu$ , $\mu^3/\lambda$, respectively. In other words, the following equalities are true,

$$E(X) = \mu \quad (24a)$$

$$\text{var}(X) = \mu^3 / \lambda \quad (24b)$$

In the situation where mean and variance are known, $\mu$ and $\lambda$ can be calculated by trivial effort,

$$\mu = E(X) \quad (24c)$$

$$\lambda = (E(X))^3 / \text{var}(X) \quad (24d)$$

Combine equations (21a), (21b), (24c) and (24d) together, we can easily get two characteristic parameters for random variable $L_{fc}$. The full-chip leakage is subjected to the inverse Gaussian distribution whose two characteristic parameters have been calculated, so we completely know about statistics of the full-chip leakage in terms of equation (23).

## 4. Experimental Setup and Results

We verify the accuracy of proposed leakage estimation algorithm using ISCAS'85 benchmark. All circuits are in implemented in 45nm technology. Technology parameters used in our experiments come from 45nm Berkeley Predictive Technology Model [17]. The circuits are synthesized with using SIS [18] with standard cell library comprised of an inverter, and NAND, NOR, AND as well as OR gates with 2, 3, 4 input pins
In our experiments, three parameters are used to model full-chip leakage variation under process variations, and they are channel length ($L_{ch}$), oxide thickness ($T_{ox}$) and threshold voltage ($V_{th}$), respectively. However, $V_{th}$ is a derived parameter, and it is dependent on channel length and channel dopant concentration [13]. For the convenience, the threshold voltage variation is regarded to be independent of channel length variation.
Now it is clear that $\mathbf{x}_{\text{variation}}$ is a random vector, containing $2N = 6$ random variables, with the first 3 of them for intra-die variations and the others for inter-die variations. Every component in $\mathbf{x}_{\text{variation}}$ is assumed to follow a univariate normal distribution, and their joint distribution is assumed to follow a multivariate normal distribution. The $3\sigma$ values of variations for $L_{ch}$, $T_{ox}$ and $V_{th}$ are all set to 50% of their nominal parameter values. Intra-die process variation contributes 60% to the full-chip variation, and inter-die process variation contributes 40%. The spatial correlation is modeled based on the process variation model.

### 4.1 Curve Fitting for Standard Cells

The full-chip leakage analysis is based on leakage from standard cells. First of all, we need to work out coefficients **A**, **b**, $c$ in the leakage model, shown in equations (8a) and (8b). For a specific standard cell, we pick up 100 samples of $\mathbf{x}_{\text{variation}}$ and run HSPICE simulations to get the leakage under each sample, then perform curve fitting to get coefficients **A**, **b**, $c$.
In order to measure how accurate the leakage model predicts leakage, we drawn 1000 samples from $\mathbf{x}_{\text{variation}}$ sample space for each standard cell $g_i \in lib$, and then use the leakage model for calculating leakage for every sample. On the other hand, HSPICE simulations are executed to get leakage for every sample, and we call it HSPICE leakage. Table 1 shows the average error of leakage model for each standard cell, compared to HSPICE leakage.

**Table 1. The average error of leakage model.**

| Standard cell name | INV1 | AND2 | AND3 | AND4 | NOR2 | NOR3 | NOR4 |
|---|---|---|---|---|---|---|---|
| Average error(%) | 0.45 | 1.86 | 3.73 | 2.85 | 1.06 | 2.07 | 3.66 |

Simulation results show that compared to HSPICE leakage, maximum average error is 3.73%, and the average error is 1.95% if using the leakage model to calculate leakage. So the leakage model is effective to calculate the leakage based on samples of the process random vector.

### 4.2 Mean and Variance of Full-chip Leakage

The leakage statistics in standard cells paves way for the full-chip leakage analysis. In this section, we are first targeting at statistics estimation of standard cells under process variations.
First 10,000 samples for $\mathbf{x}_{\text{variation}}$ are drawn for each standard cell in terms of $\mathbf{x}_{\text{variation}}$ distribution, and then get the mean value and variance of the leakage.
After the mean and variance of the standard cell is ready, we get the mean value and variance of full-chip leakage by equations (21a) and (21b). On the other hand, we also perform Monte Carlo (MC) simulation to get the full-chip leakage for comparison. Monte Carlo simulation take hours to finish for a single benchmark circuit, while the proposed algorithm can provide results in a minute. And the proposed algorithm is over 1000X faster than Monte Carlo simulation. The simulation results are shown in Table 2.
By observing the experimental results from table 2, we see the estimation errors in mean and variance are no more than -2.73%, and -5.09%, respectively.

**Table 2. Mean and variance of Full-chip Leakage: Monte Carlo vs. the proposed algorithm.**

| Circuit Name | Monte Carlo | | Proposed algorithm | | | |
|---|---|---|---|---|---|---|
| | mean ($\mu$A) | variance ($\mu A^2$) | mean ($\mu$A) | Error (%) | variance ($\mu A^2$) | Error (%) |
| C432 | 1.81 | 1.14 | 1.76 | -2.73 | 1.19 | 4.77 |
| C880 | 3.09 | 3.03 | 3.01 | -2.50 | 2.93 | -3.28 |
| C1355 | 4.58 | 1.93 | 4.50 | -1.76 | 1.92 | -0.39 |
| C1908 | 5.92 | 4.62 | 5.89 | -0.53 | 4.56 | -1.33 |
| C2670 | 7.27 | 4.67 | 7.29 | 0.32 | 4.43 | -5.09 |
| C3540 | 10.3 | 9.42 | 10.04 | -2.49 | 9.05 | -3.89 |
| C5312 | 15.8 | 15.29 | 15.95 | 0.93 | 15.33 | 0.29 |
| C6288 | 21.7 | 33.06 | 21.77 | 0.32 | 33.93 | 2.63 |
| C7552 | 25.7 | 27.98 | 25.93 | 0.89 | 27.16 | -2.92 |

## 4.3 Leakage Distribution

In this section, we will compare the leakage distribution obtained by the proposed algorithm against the one from Monte Carlo (MC) simulation.

We know the leakage is following an inverse Gaussian distribution, so before plotting its probability density curve, all we should do is to compute its two characteristic parameters $\mu$ and $\lambda$, which is easily achieved by making use of the mean value and variance, shown in equations (24c) and (24d). After that, the probability density curve is plotted in terms of equation (23).

For the sake of convenience, take benchmark circuit C1355 as an example, two probability density curves is shown in Figure 1. One is from our algorithm, the other from Monte Carlo simulation, which is used for a benchmark.

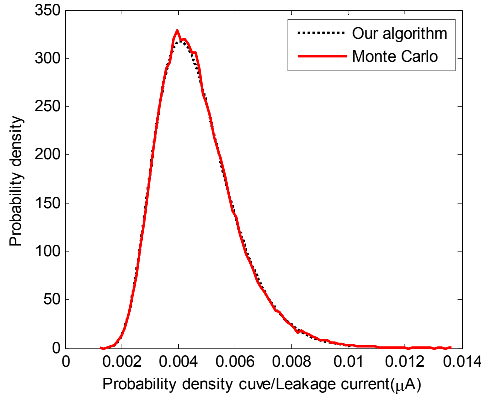


**Figure 1. The probability density curve for C1355: the proposed algorithm vs. Monte Carlo .**

From the plot, we can see the two curves are nearly overlapping with each other, so our algorithm works well for leakage distribution estimation. However, that is a qualitative consequence; in order to measure how close these two curves are to each other, we define a new measurement $G$ as,

$$G = \int_{x>0} \frac{|f_{MC}(x) - f_{esti}(x)|}{f_{MC}(x)} f_{MC}(x)dx = \int_{x>0} |f_{MC}(x) - f_{esti}(x)| dx \quad (25)$$

where $f_{MC}(x)$, $f_{esti}(x)$ are the probability density function estimated from Monte Carlo simulation and the proposed algorithm, respectively.

Parameter $G$ measures the average error of estimated probability density function (*pdf*) $f_{esti}(x)$, compared against $f_{MC}(x)$. In the case of benchmark circuit C1355, $G$ is 1.85 %. We report $G$ values for all benchmark circuits in Table 3.

Table 3 shows that using the inverse Gaussian distribution as an estimate for leakage distribution, the error is no more than 5.33%.

**Table 3. The average error of pdf estimation.**

| Ckt Name | C432 | C880 | C1355 | C1908 | C2670 | C3540 | C5312 | C6288 | C7552 |
|---|---|---|---|---|---|---|---|---|---|
| $G$(%) | 5.33 | 4.87 | 1.85 | 3.70 | 1.55 | 2.71 | 1.84 | 3.82 | 2.95 |

Therefore, the proposed algorithm is effective in estimate the full-chip leakage estimation under process variations.

## 5 Conclusion

In this paper, we have proposed a probability-based full-chip leakage estimation algorithm. First of all, the process variations are modeled as a process random vector, the first half of whose components denote the intra-die variations, and the second half for the inter-die variations. Based on the assumption that each component in process random vector is a Gaussian random variable, we have derived that the leakage in every standard cell under process variations is subjected to an inverse Gaussian distribution. By further derivation, we get a significant consequence that the full-chip leakage is also following an inverse Gaussian distribution under process variation. Therefore, after knowing the mean value and variance of full-chip leakage, we have the complete information about the full-chip leakage under process variations.

Experimental results show that the proposed leakage estimation algorithm is fast and effective to capture the statistics of the leakage under process variations. The proposed algorithm does not require the layout information, so it can also be used for pre-layout leakage analysis as well.

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